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**Remarks**

This is an amendment under 37 CFR § 1.116. The purpose of this amendment is to put the claims in better form for appeal. The amendments and specific arguments in this amendment, to the extent they were not presented earlier, are now presented because they are necessitated by the new arguments of anticipation and obviousness set forth by the Examiner in the official action dated 9 February 2005. The applicants respectfully submit that these amendments do not raise new issues and do not require any further searching.

Following this amendment, claims 1-20 are active in the application.

**I. CLAIM REJECTIONS UNDER 35 USC § 102(b)****A. Claims 1, 2, 4, 6, 7, and 10**

Claims 1, 2, 4, 6, 7, and 10 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 5,986,885 of Wyland. The official action alleges that the limitation, "for attachment of the die with a major surface of the die in contact therewith," represents an intended use. The applicants respectfully disagree, but to advance prosecution of the application have amended Claim 1 to recite a more explicit structural limitation.

The applicants respectfully submit that Wyland's metallization 61, alleged in the official action to correspond to the die mounting pad recited in Claim 1, cannot accurately be described as "dimensioned to accommodate the die with a major surface of the die in contact therewith" as recited in Claim 1 as now amended.

Accordingly, the applicants respectfully submit that Claim 1 as now amended, and claims 2-9 that depend on Claim 1, are all patentable.

**B. Claim 6**

With reference to claim 6, the official action alleges that Wyland discloses a bonding pad, citing "(right side, Figure 6) (61) located "on" one of the major surfaces." This differs from the rejection set forth in the previous official action mailed on 23 August 2004 in which Wyland's *die bonding pad 31* was alleged to correspond to the bonding pad recited in Claim 6. In its Response to Arguments, the official action states that the applicants were incorrect and refers to

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"bonding pad (61)." However, the applicants respectfully submit that the previous official action referred to element 31, i.e., to die bonding pad 31, and not to element 61, i.e., metallization 61, as now alleged.

The applicants have amended Claim 6 to recite: "a bonding pad smaller in area than the die mounting pad, the bonding pad located on the one of the major surfaces." The applicants respectfully submit that Wyland's metallizations 61 to which die 30 is attached are substantially similar in area, as would be expected given that the die is attached to each metallization by means of a flip-chip connection. The applicants therefore respectfully submit that, in Wyland's semiconductor package, the metallization 61 alleged to correspond to the bonding pad recited in claim 6 cannot accurately be said to be smaller in area than the metallization 61 alleged in the rejection of Claim 1 to correspond to the die mounting pad recited in Claim 1.

Accordingly, the applicants respectfully submit that Claim 6 as now amended is patentable for this additional reason, and Claims 7-10 that depend on Claim 6 are also patentable.

#### *C. Claims 11, 12, 16, and 17*

Claims 11, 12, 16, and 17 are rejected under 35 USC § 102(b) as being anticipated by United States patent no. 6,084,295 of Horiuchi et al. (*Horiuchi*).

The official action alleges that bonding pad 22 corresponds to the mounting pad recited in claim 11. The applicants respectfully thank the Examiner for clearly identifying the element alleged to correspond to the mounting pad. The prior official action did not indicate that Horiuchi's bonding pad 22 corresponded to the mounting pad. In responding to the prior official action, the applicants took the reference to "upper surface" to refer to the upper surface of substrate 5 rather than to the upper surface of bonding pad 22. It appears that this is not what the Examiner intended.

The applicants respectfully submit that bonding pad 22 cannot accurately be said to correspond to "a conductive mounting pad located on one of the major surfaces" as recited in the original version of Claim 11. Horiuchi shows bonding pad 22 located in a region of substrate 5 outside that occupied by semiconductor chip 10. The original version of Claim 11 recites in part: "a semiconductor die attached to the mounting pad." The applicants respectfully submit that chip

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10 cannot accurately be described as attached to bonding pad 22.

Moreover, Horiuchi shows vias 16 underlying chip 10. Figure 1 shows the ends of vias 16 adjacent chip 10 lying flush with the surface of substrate 5. The applicants therefore respectfully submit that the ends of vias 16 therefore cannot accurately be said to be "on" the major surface of the substrate. The official action provides no indication of where may be found in Horiuchi's disclosure a teaching that bonding pads similar to bonding pads 22 exist under chip 10. The applicants have been unable to find such teaching. Figures 7(a) and 7(c) referred to the prior official action show structures of pads to which bonding wires 20 are attached, and not of the vias underlying chip 10.

Nevertheless, to advance prosecution of the application and to conform Claim 11 with Claim 1, the applicants have amended Claim 11 to recite: "located on one of the major surfaces, a conductive die mounting pad dimensioned to accommodate the semiconductor die" and "in which the semiconductor die is mounted on the die mounting pad with a major surface thereof in contact with the mounting pad." The applicants respectfully submit that Horiuchi's device lacks any element described by the quoted elements of Claim 11 as now amended.

Accordingly, the applicants respectfully submit that Claim 11 as now amended is patentable. The applicants further submit that Claims 12-19 that depend on Claim 11 are patentable due to the patentability of Claim 11.

## II. CLAIM REJECTIONS UNDER 35 USC § 103(a)

### A. *Claims 3 and 8*

Claims 3 and 8 are rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of *Innovative PCB Reinforcement, ELECTRONIC PACKAGING AND PRODUCTION*, 1 (1997) (the Article).

The official action states that Wyland does not disclose a substrate material composed of epoxy laminate and looks to ELECTRONIC PACKAGING AND PRODUCTION for a disclosure of this material. The official action states:

Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of Electronic Packaging and Technology with Wyland to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5 th para.).

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The Article discloses mounting thin, small outline integrated circuit packages (TSOPs) on a multilayer reinforced epoxy laminate printed circuit board. The TSOPs are composed of a semiconductor die attached to a metal lead frame. The die and part of the lead frame are encapsulated. Portions of the lead frame remote from the die are attached to the printed circuit board by solder. The use of an epoxy laminate as the material of the printed circuit board was apparently motivated by the need for the printed circuit board to match the coefficient of thermal expansion of the TSOPs to increase the reliability of solder connections between the TSOPs and the printed circuit board.

The structure of Wyland's device is different: a semiconductor die 30 is flip-chip mounted on first circuitry metallizations 61 located on the surface of a substrate 60.

The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of the semiconductor die 30 of Wyland's semiconductor device are so different from those of a TSOP attached to a printed circuit board that such person would consider any teaching set forth in the Article with respect to the printed circuit board material as inapplicable to choosing the substrate material of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that the cited references lack any teaching or suggestion that could properly be regarded as providing a motivation for a person of ordinary skill in the art to combine the references in the manner proposed in the official action.

The official action states that multilayer laminate boards are extremely well known in the art and widely utilized. The applicants do not dispute this. However, the applicants respectfully remind the Examiner that the fact that multi-layer boards are known does not make it obvious to modify Wyland's semiconductor device to incorporate a multilayer board absent a teaching or suggestion in the cited references that can properly be regarded as a motivation for a person of ordinary skill in the art to make such modification. The applicants respectfully submit that the passage of the Article cited in the official action does not rise to this level. It simply describes an advantage that arises in the specific circumstance in which TSOPs are mounted on a PC11 printed circuit board. The applicants have been unable to find anything in the Article that teaches or suggests that this advantage would be obtained in the context of Wyland's semiconductor

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package in which a semiconductor die is flip-chip mounted on a substrate. The applicants have been unable to find anything in Wyland's disclosure that teaches or suggests that his semiconductor package has problems with solder joint reliability.

Moreover, the official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to attempt to modify Wyland's semiconductor package in the manner suggested in the official action.

Additionally, the applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, would still lack a die mounting pad, for the reason set forth above with reference to Claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 3 and 8.

The applicants therefore respectfully submit that the rejection of claims 3 and 8 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

#### *B. Claims 5 and 10*

Claims 5 and 10 are rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of Wilson et al. (**HANDBOOK OF MULTILEVEL METALLIZATION FOR INTEGRATED CIRCUITS**, 868-872 (*Wilson*)).

The official action indicates that Wyland does not disclose a conductive interconnecting element (via) comprising tungsten and looks to Wilson for a teaching of conductive interconnect elements (vias) composed of tungsten. The official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Wyland to reduce costs (p. 868, lines 11 - 12) and reduce signal delays (p. 872, Figure 10).

The cited passage of Wilson's disclosure describes the advantages of CVD tungsten contacts and via plugs in integrated circuits. The official action proposes to apply Wilson's teachings to the choice of the material to fill through holes 62 extending through the substrate 60 of Wyland's semiconductor package. The applicants respectfully submit that the substrate of a

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semiconductor package cannot accurately be referred to as an integrated circuit. Accordingly, the applicants respectfully submit that the person of ordinary skill in the art would regard Wilson's teaching with respect to the material of the interlayer plugs of an integrated circuit inapplicable to the choice of material to fill the through holes 62 of Wyland's semiconductor package. Accordingly, the applicants respectfully submit that the cited passage of Wilson's disclosure does not provide a sufficient motivation for a person of ordinary skill in the art to make the combination of references proposed in the official action.

Moreover, the applicants respectfully submit that Wilson is non-analogous art and hence, is not a valid reference with respect to the invention claimed in Claims 5 and 10. The invention claimed in Claims 5 and 10 relates to a packaging device for a semiconductor die. Wilson's disclosure relates to the structure of the semiconductor die itself. The *Manual of Patent Classification* classifies Horiuchi's semiconductor device, which is analogous prior art, in class 257, subclass 690, whereas integrated circuit vias appear to fall into class 438.

The sentence that includes the passage of Wilson's disclosure cited in the official action as constituting a motivation reads: "There are also attempts to use a selective CVD tungsten because of the potential process simplification and cost savings." The applicants respectfully submit that this passage of Wilson's disclosure does not indicate whether the attempts have been successful or that the potential cost savings have been achieved. Moreover, the applicants have been unable to find any teaching in the cited passage or elsewhere in Wilson's disclosure that teaches or suggests that tungsten provides a cost advantage in an application other than in an integrated circuit. The applicants respectfully remind the Examiner that obviousness is not established if a person of ordinary skill might find it *obvious to try* to modify the teaching of one reference in accordance with the teachings of another. "[T]his is not the standard of 35 USC § 103." *In re Geiger*, 815 F2d 686, 688, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987).

The official action additionally cites Wilson's Figure 10 as demonstrating that tungsten interconnects and inter-layer plugs reduce signal delays, and thus provide a motivation. The applicants respectfully submit that Figure 10 demonstrates that, with respect to signal delay in an integrated circuit, tungsten performs marginally better than aluminum but performs significantly worse than copper. The applicants therefore respectfully submit that, if anything, Wilson's

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Figure 10 teaches away from using tungsten.

Moreover, the applicants have been unable to find anything in Wyland's disclosure that teaches or suggests that his semiconductor package is costly to manufacture and/or suffers from problems with signal delay that would provide a person of ordinary skill in the art with a motivation to look outside Wyland's disclosure for a solution to such problems.

The official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Wyland's semiconductor package proposed in the official action.

Finally, the applicants respectfully submit that Wyland's semiconductor package, modified as proposed in the official action, lacks the die mounting pad recited in Claim 1 on which Claims 5 and 10 depend for the reasons set forth above with reference to Claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest all the claim limitations recited in Claims 5 and 10.

The applicants therefore respectfully submit that the rejection of claims 5 and 10 is improper because the prima facie case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the rejection be withdrawn.

### *C. Claim 9*

Claim 9 is rejected under 35 USC § 103(a) as being unpatentable over Wyland as applied to Claims 1, 2, 4, 6, 7 and 10 in view of United States patent no. 6,620,720 of Moyer et al. (*Moyer*).

The official action indicates that Wyland does not disclose that the bond pad is composed of copper and looks to Moyer at (col. 2, lines 48 - 49) for a disclosure of a copper contact (bond) pad (31) (Figure 1) formed on the silicon substrate for either wire bonding or solder bump bonding. The official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer with Wyland to provide a contact (bond) pad of low cost and high conductivity (Moyer, col. 1, lines 41 - 43).

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The applicants acknowledge that the cited passage of Moyer's disclosure describes the advantages of using copper as the material of the interconnects of an integrated circuit. However, in the lines following the cited passage of Moyer's disclosure, Moyer discloses some of the many difficulties of using copper as the material of the interconnects of an integrated circuit. Moyer discloses a solution to the problems of using copper to form the bonding pads of an integrated circuit. Moyer's solution involves the deposition of several additional layers over the copper bonding pad. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the main motivation for adopting copper interconnects in integrated circuits, namely, maintaining low-resistance connections despite ever-decreasing feature sizes, does not apply to selecting the material of the bonding pads of Wyland's semiconductor package. The applicants respectfully submit that this absence of a motivation to use copper, together with Moyer's disclosure of the additional difficulties of using copper, means that such person would have no motivation to adopt the teaching set forth in Moyer's disclosure with respect to the material of the bonding pads of Wyland's semiconductor package.

The applicants additionally submit that Moyer is non-analogous art and, hence, is not a valid reference with respect to the invention claimed in Claim 9. The invention claimed in Claim 9 relates to the structure of a packaging device for a semiconductor die. Moyer's disclosure relates to structures for the bonding pads of an integrated circuit having copper interconnects. The *Manual of Patent Classification* classifies Horiuchi's semiconductor device, which is analogous prior art, in class 257, subclass 690, whereas it classified Moyer's disclosure in class 438, subclass 612.

The official action asserts that col. 1, lines 41-43, of Moyer's disclosure provides more than sufficient motivation to use Moyer's copper contact pad in Wyland's semiconductor package. The applicants do not dispute that the cited passage of Moyer's disclosure teaches the desirability of using copper as an interconnect material in an integrated circuit. However, the portion of Wyland's semiconductor package the Examiner is proposing to modify is metallization 61 that forms part of the semiconductor package and is not part of semiconductor die 30. The applicants have been unable to find anything in Moyer's disclosure that teaches or suggests the desirability of making an element of a semiconductor package corresponding to

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Wyland's metallization 61 of copper.

Moreover, the applicants respectfully submit that the portion of Moyer's disclosure cited in the official action quotes is taken out of the context of the discussion of the problems of using copper as an interconnect material in integrated circuits that immediately follows the cited passage. The applicants respectfully submit that this portion of Moyer's disclosure would discourage a person of ordinary skill in the art from using copper as the interconnect material of an integrated circuit absent the compelling reason of high-frequency performance. The applicants further submit that Moyer is silent with respect to the suitability of copper in applications such as Wyland's metallization 61, and that this would further discourage the person of ordinary skill in the art from making the modification proposed in the official action. Moreover, in view of the caveats uttered by Moyer about the problems of using copper, Moyer's disclosure as a whole cannot reasonably be regarded as providing the person of ordinary skill in the art with a reasonable expectation of success in the event such person were to attempt to perform the proposed modification of Wyland's semiconductor package. Finally, the applicants note that they have been unable to find anything in Wyland's disclosure that teaches or suggests that the performance of his semiconductor package is unsatisfactory at high frequencies. Such teaching might motivate the person of ordinary skill in the art to ignore Moyer's teaching with regard to the difficulties of using copper, but no such teaching or suggestion can be found.

The official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Wyland's semiconductor package proposed in the official action.

Additionally, the applicants submit that Wyland's semiconductor package, modified as proposed in the official action, would still lack a die mounting pad for the reason set forth above with reference to Claim 1. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claim 9.

The applicants therefore respectfully submit that the rejection of claim 9 is improper because the *prima facie* case of obviousness set forth in the official action does not meet the requirements set forth in MPEP § 2143. The applicants therefore respectfully request that the

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rejection be withdrawn.

*D. Claims 13 and 18*

Claims 13 and 18 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of *Electronic Packaging and Production* (the Article).

The official action indicates that Horiuchi does not disclose a substrate material composed of epoxy laminate and looks to *Electronic Packaging and Production* for a disclosure of this material. The official action states:

Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the disclosures of *Electronic Packaging and Technology* with Horiuchi et al. to obtain a device with increased reliability and reduced fatigue at joints (p. 1, left column, 5th para.).

The disclosure of the Article is described above with reference to claims 3 and 8.

The applicants respectfully submit that structure of Horiuchi's device package is different than that of the TSOPs discussed in the Article: in Horiuchi's device package, semiconductor die 10 is attached directly to the surface of substrate 5. The applicants respectfully submit that the person of ordinary skill in the art would appreciate that the thermal expansion considerations of Horiuchi's semiconductor device are so different from those of a TSOP attached to a printed circuit board that such person would consider any teaching set forth in the Article with respect to printed circuit board material as inapplicable to choosing the substrate material of Horiuchi's semiconductor device. Accordingly, the applicants respectfully submit that the rationale set forth in the official action for combining the cited references does not meet the requirements set forth in MPEP § 2143.

Additionally, the applicants respectfully submit that Horiuchi's semiconductor device, modified as proposed in the official action, would still lack "located on one of the major surfaces, a conductive die mounting pad dimensioned to accommodate the semiconductor die" and "in which the semiconductor die is mounted on the die mounting pad with a major surface thereof in contact with the mounting pad." for the reasons set forth above with reference to claim 11. Accordingly, the applicants respectfully submit that the proposed combination of references does not teach or suggest every element of claims 13 and 18.

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The official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Horiguchi's semiconductor device proposed in the official action.

Accordingly the applicants respectfully submit that the rejection of claims 13 and 18 is improper because the official action does not set forth a prima facie case of obviousness that complies with the requirements set forth in MPEP § 2143.

*E. Claims 15 and 20*

Claims 15 and 20 are rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as applied to Claims 11, 12, 16, and 17 in view of Wilson.

The official action indicates that Horiuchi does not disclose a conductive interconnecting element (via) comprising tungsten and looks to Wilson for a disclosure of this material. The official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Horiuchi et al. to reduce costs (p. 868, lines 11-12) and reduce signal delays (p. 872, Figure 10).

For reasons corresponding to those described above with reference to Claims 5 and 10, the applicants respectfully submit that the rejection of claims 15 and 20 is improper because the prima facie case of obviousness set forth in the official action does not comply with the requirements set forth in MPEP § 2143. Specifically, the official action does not set forth a motivation that complies with the requirements set forth in MPEP § 2143, the official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Horiuchi's semiconductor device proposed in the official action and the proposed combination of references does not teach or suggest all the claim limitations.

*F. Claim 19*

Claim 19 is rejected under 35 USC § 103(a) as being unpatentable over Horiuchi as

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applied to Claims 11, 12, 16, and 17 in view of Moyer and Wyland.

The official action states that Horiuchi does not disclose that the mounting pad, bond pad, and connecting pad are composed of copper and looks to Wyland for a teaching of a mounting pad and a connecting pad (63) composed of copper and looks to Moyer for a teaching of a copper contact (bond) pad (13) (Figure 1) formed on the silicon substrate for either wire bonding or solder bump bonding. The official action states:

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moyer et al. and Wyland with Horiuchi et al. to provide a metallic contact structures of low cost and high conductivity (Moyer et al., col. 1, lines 41-43).

For reasons corresponding to those described above with reference to Claim 9, the applicants respectfully submit that the rejection of claim 19 is improper because the *prima facie* case of obviousness set forth in the official action does not comply with the requirements set forth in MPEP § 2143. Specifically, the official action does not set forth a motivation that complies with the requirements set forth in MPEP § 2143, the official action does not indicate where in the cited references may be found a teaching or suggestion that would provide a person of ordinary skill in the art with a reasonable expectation of success in the event such person were to undertake the modification of Horiuchi's semiconductor device proposed in the official action and the proposed combination of references does not teach or suggest all the claim limitations.

The applicants respectfully request that the amendments set forth above be entered and that Examiner reconsider the rejection of the rejected claims. The applicants believe that the application as now amended is in condition for allowance, and respectfully request such favorable action. If any matters remain outstanding in the application, the Examiner is respectfully invited to telephone the applicant attorney at (650) 485-3015 so that these matters may be resolved.

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Respectfully submitted,  
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